REMARKS

This application has been further reviewed in light of the Office Action dated September 6, 2006. Claims 1 to 12 and 14 to 16 remain pending in the application. Claims 1, 5, 6, 10, 14 and 15 are the independent claims herein. Reconsideration and further examination are respectfully requested.

Claims 1 to 8, 10 and 14 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,961,616 (Wakasugi) in view of U.S. Patent No. 5,818,603 (Motoyama), Claims 15 and 16 were rejected under § 103(a) over U.S. Patent No. 5,831,683 (Matsumoto) in view of Motoyama, Claim 9 was rejected under § 103(a) over Wakasugi in view of Motoyama and further in view of U.S. Patent No. 6,175,603 (Chapman), and Claims 11 and 12 were rejected under § 103(a) over Wakasugi in view of Motoyama and further in view of U.S. Patent No. 6,453,272 (Slechta). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention relates to an interface apparatus (e.g., in a printer) fetching and outputting information input from an external apparatus. According to the invention, when information is input from the external apparatus, and a change is detected in the input information, the input information is fetched from the external apparatus. Then, a determination is made whether or not the fetched information is the same as information fetched a previous time. If not, then the information is fetched. If so, the fetched information is output (printed).

Referring specifically to the claims, amended independent Claim 1 is directed to an interface apparatus for inputting information from an external apparatus, comprising a first circuit for, in a case where there is a change in information input from

the external apparatus, fetching the information after an elapse of a predetermined time, and a second circuit for determining whether the information fetched by the first circuit is the same as information fetched by the first circuit a previous time, and when the information fetched by the first circuit is not the same as the information fetched by the first circuit the previous time, outputting the fetched information, and wherein, when the information fetched by the first circuit is the same as the information fetched by the first circuit the previous time, the second circuit does not output the fetched information.

Independent Claims 5, 6 and 10 are directed to a printer, a method, and a printing method, respectively, and substantially correspond to Claim 1.

Independent Claim 14 includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an external apparatus, comprising a change detector for detecting a change in information input from the external apparatus and outputting a reset upon the detection of the change, a timer for inputting the reset output by the change detector and outputting a trigger after an elapse of a predetermined time from the input of the reset, a latch for inputting the trigger output by the timer and fetching information input from the external apparatus upon the input of the trigger; and a logical filter for determining whether the information fetched by the latch is the same as information fetched by the latch a previous time, and when the information fetched by the latch is not the same as the information fetched by the latch the previous time, outputting the fetched information, and wherein, when the information fetched by the latch is the same as the information fetched by the latch the previous time, the logical filter does not output the fetched information.

Independent Claim 15 also includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an external apparatus, comprising a timer for timing a predetermined time, a comparator for making a comparison between a length of a low level state in information input from the external apparatus within the predetermined time timed by the timer, and a length of a high level state in the information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the comparison shows that the length of the high level state is longer than the length of the low level state, and a logical filter for determining whether information indicated by the signal output by the comparator is the same as information indicated by the signal output by the comparator a previous time, and when the information indicated by the signal output by the comparator is not the same as the information indicated by the signal output by the comparator the previous time, outputting the indicated information, and wherein, when the information indicated by the signal output by the comparator is the same as the information indicated by the signal output by the comparator the previous time, the logical filter does not output the indicated information.

The applied, alone or in any permissible combination, is not seen to disclose or to suggest the features of the present invention. With regard to Claims 1, 5, 6 and 10, the applied art is not seen to disclose or to suggest at least the features of determining whether information fetched by a first circuit after a predetermined time has elapsed when there is a change in input information from an external apparatus is the same as information fetched by the first circuit a previous time, and when the information fetched

by the first circuit is not the same as the information fetched the previous time, outputting the fetched information, and wherein, when the information fetched by the first circuit is the same as the information fetched the previous time, the second circuit does not output the fetched information.

Similarly, with regard to Claim 14, the applied art is not seen to disclose or to suggest at least the feature of a logical filter determining whether information fetched by a latch upon input of a trigger is the same as information fetched by the latch a previous time, and when the information fetched by the latch is the not same as the information fetched the previous time, outputting the fetched information, and wherein, when the information fetched by the latch is the same as the information fetched the previous time, the logical filter does not output the fetched information.

Along the same lines, with regard to Claim 15, the applied art is not seen to disclose or to suggest at least the feature of a logical filter determining whether information indicated by a signal output by a comparator is the same as information indicated by the signal output by the comparator a previous time, and when the information indicated by the signal output by the comparator is not the same as the information indicated by the signal output by the comparator the previous time, outputting the indicated information, and wherein, when the information indicated by the signal output by the comparator is the same as the information indicated by the signal output by the comparator the previous time, the logical filter does not output the indicated information.

The Office Action admits that Wakasugi fails to teach the various foregoing features of the invention. However, the Office Action cites Motoyama as allegedly making up for Wakasugi's deficiencies.

Motoyama does not disclose or suggest any means corresponding to the second circuit (step) in the present invention. As apparent from the claims, the second circuit (step) is characterized by eliminating a noise by comparing the information fetched a previous time and the information fetched this time with each other. In particular, if the information fetched the previous time and the information fetched this time are judged to be the same, the information fetched this time is not output so as to eliminate the noise. In Motoyama, it is first judged whether a protocol identifier exists. Then, if the protocol identifier exists, it is judged whether an actual format of subsequent data is correct, based on format data corresponding to the relevant protocol identifier. That is, in Motoyama, it is necessary to handle the format data independently of the subsequent data. Meanwhile, in the present invention, a noise can be eliminated without previously managing such format data. On the other hand, in Motoyama, if the format data coincides with the subsequent data, the data is judged to be in conformity with the protocol. However, in the present invention, if the information fetched the previous time and the information fetched this time are not the same, the information fetched this time is judged to be in conformity with the protocol. This is a point completely different from Motoyama. Thus, the proposed combination of Wakasugi and Motoyama is not seen to teach the features of the invention.

The other art of record, namely Matsumoto, Chapman, and Slechta are not seen to make up for the deficiencies of Wakasugi and Motoyama, and any permissible combination of the references is not seen to result in the invention.

In view of the foregoing deficiencies of the applied art, independent Claims 1, 5, 6, 10, 14 and 15, as well as the claims dependent therefrom, are believed to be in condition for allowance.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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